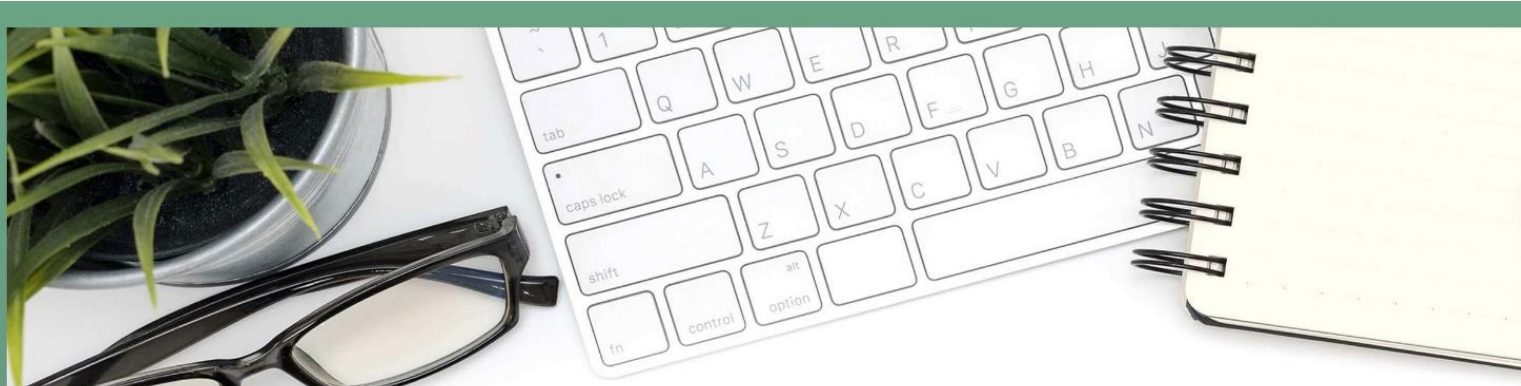

JEE Main Physics

Short Notes

Semiconductor Electronics

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Semiconductor Electronics is an important topic from JEE Main / JEE Advanced Exam Point of view. Every year there are 1-3 questions asked from this topic. This short notes on Semiconductor Electronics will help you in revising the topic before the JEE Main & IIT JEE Advanced Exam.

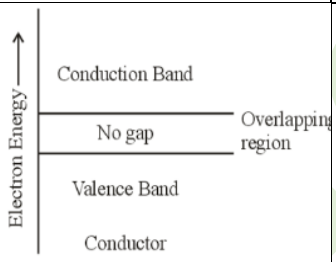
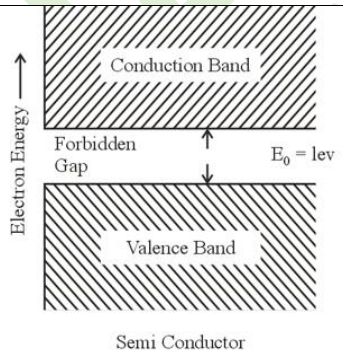
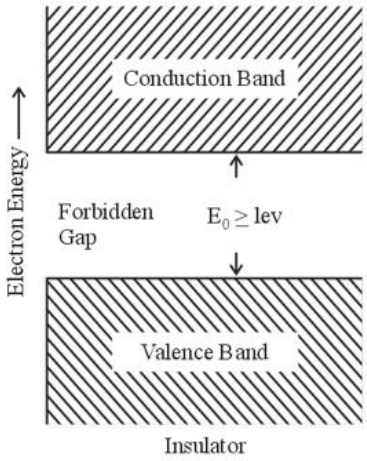
Semiconductor Electronics

Energy Band

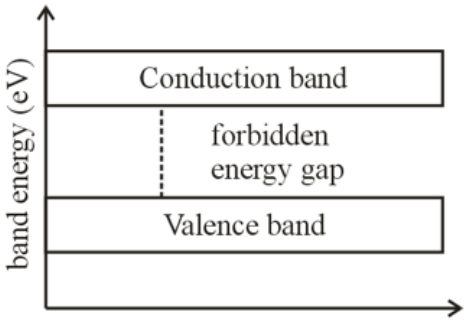
Energy band is defined as the range of energy possessed by an electron in a solid. There are two types of energy band in solids.

Valence Band-It is defined as the range of energy possessed by valence electron. This band is always filled by electrons.

Conduction Band-It is defined as the range of energy possessed by the free electron.

Properties	Conductor	Semiconductor	Insulator
Flow of current	Only due to free electrons	Due to electrons and holes	No current flow
Energy band diagram			
Temperature Coefficient of resistance (α)	Positive	Negative	Positive (Slightly)
Example	Pt, Al, Cu, Ag,..	Ge, Si, GaAs,..	Wood, plastic, ..

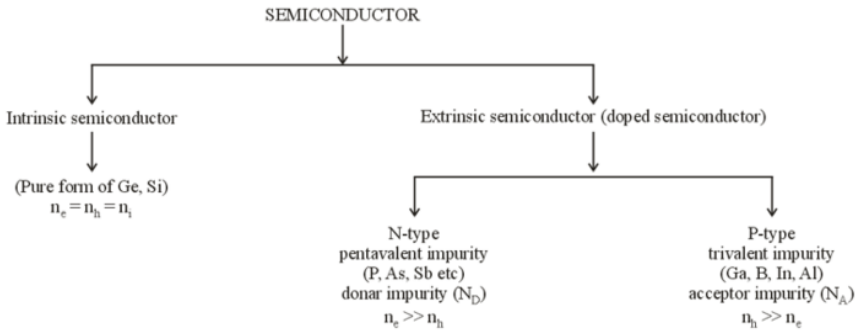
Forbidden Energy gap- The energy gap between the conduction band and valence band, where no free electron can exist. As temperature increases, the forbidden energy gap decreases (very slightly).



Classification of Conductor, Insulator and semiconductor

On the basis of electrical conductivity and energy bands, the solids are broadly classified into three categories- Conductors, Semiconductors, and Insulator

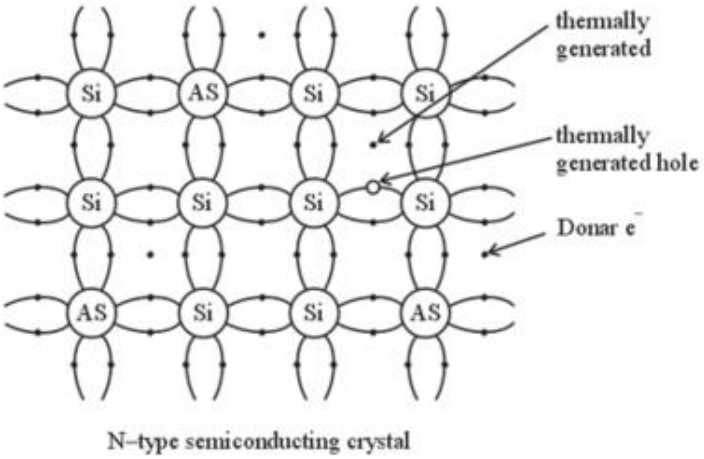
Semiconductor



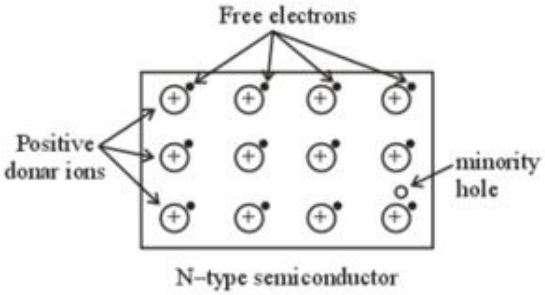
Extrinsic Semiconductor

(A) N-type semiconductor

When a pure semiconductor (Si or Ge) is doped by pentavalent impurity (P, As, Sb, Bi) then four electrons out of the five valence electrons of impurity take part, In covalent, with four silicon atoms surrounding it and the fifth electron is set free. These impurity atoms which donate free e for conduction are called as Donor impurity (N_0) Due to donor impurity free e^- increases very much so it is "N" type semiconductor. By semiconductor free e^- are called as "majority" charge carriers and "holes" are called as "minority" charge carriers.



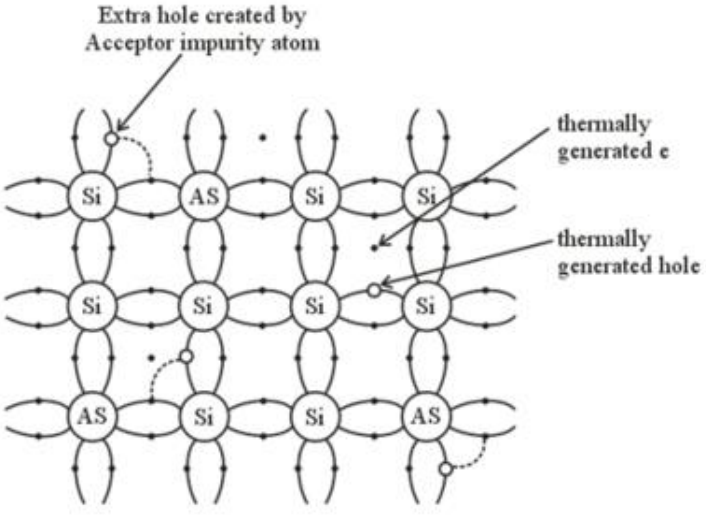
N–type semiconducting crystal



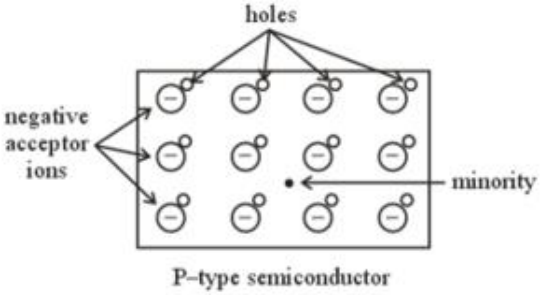
N–type semiconductor

(B) P-type Semiconductor

When a pure semiconductor (Si or Ge) is doped by trivalent impurity (B, Al, In, Ga) then outer most three electrons of the valence band of impurity take part, in covalent bonding with four silicon atoms surrounding it and except one electron from the semiconductor and make the hole in a semiconductor. These impurity atoms which accept bonded e^- from valance band are called as Acceptor impurity (N_A). Here holes increases very much so it is called as "P" type semiconductor and impurity ions known as "Immobile Acceptor negative Ion". In P–type semiconductor free e^- are called as minority charge carries and holes are called as majority charge carriers.



P–type semiconducting crystal



P–type semiconductor

Mass Action Law

The generation of free e^- and the hole in the semiconductor is taken place due to thermal effect.

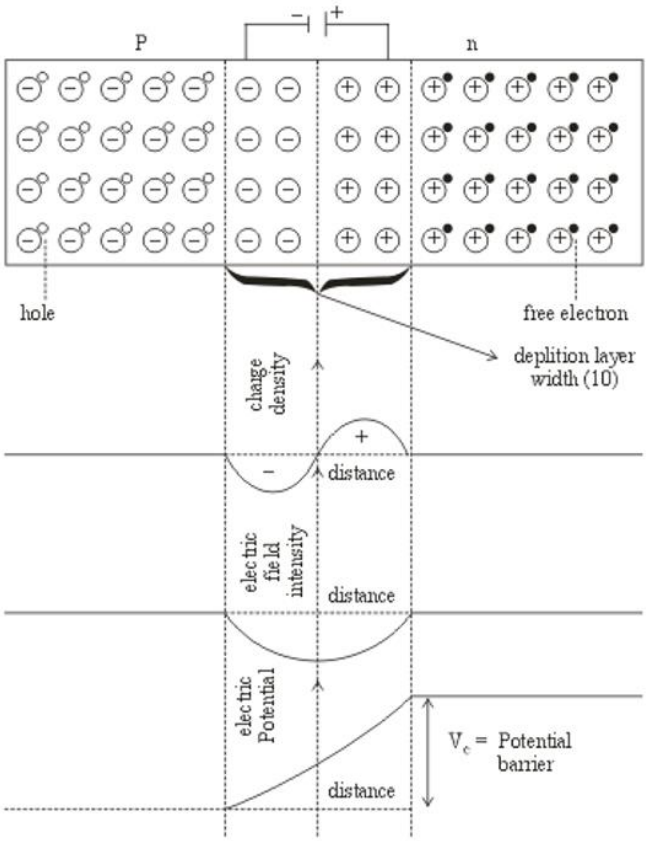
Under thermal equilibrium, the product of the concentration 'n_e' of free electrons and the concentration n_h of holes is a constant and it is independent of the amount of doping by acceptor and donor impurities.

Thus, from mass action law $\boxed{n_e \times n_h = n_i^2}$

PN junction

Given diagram shows a P–N junction immediately after it is formed P region has mobile majority holes and immobile negatively charged impurity ions. N region has mobile majority free electrons and immobile positively charged impurity ions. Due to concentration difference diffusion of holes starts from P to N side and diffusion of e^- s starts N to P side.

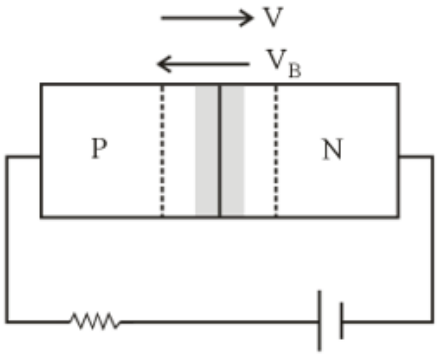
Due to this a layer of only positive (in N side) and negative (in P–side) started to from which generate an electric field (N to P side) which oppose diffusion process, during diffusion magnitude of electric field increases due to this diffusion it gradually decreased and ultimately stopes. The layer of immobile positive and negative ions, which have no free electrons and holes called as **depletion layer** as shown in the diagram.



Forward Bias

In forward bias P–side of the diode is connected to the positive terminal of battery and N-side is connected to the negative side of the battery.

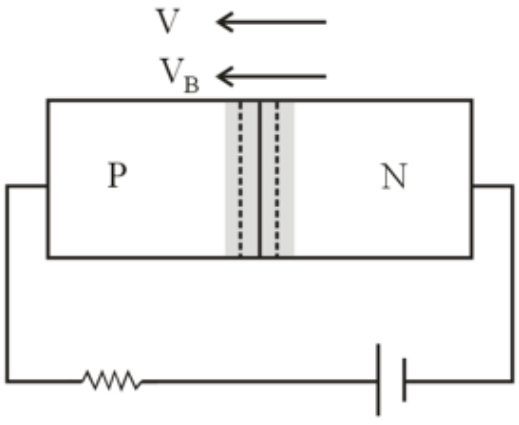
The applied voltage is opposite to the junction barrier potential. Due to this effective potential barrier decreases, junction width also decreases, so more majority carriers will be allowed to flow across the junction. It means the current flow in principally due to majority charge carriers and it is in the order of mA called as forward bias.



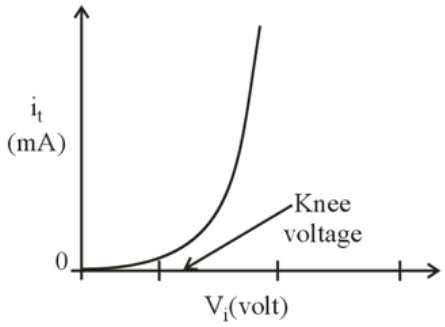
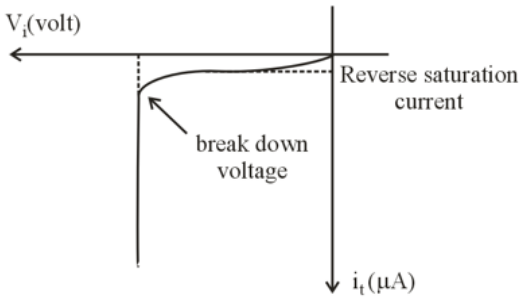
Reverse Bias

In reverse bias P–side of the diode is connected to the negative terminal of battery and N-side is connected to the positive side of the battery.

The applied voltage is in same direction as the junction barrier potential. Due to this effective potential barrier increases junction, width also increases, so no majority carriers will be allowed to flow across junction. Only minority carriers will be drifted. It means the current flow in principally due to minority charge carriers is very small (in the order of mA). This bias is called as reversed Bias.



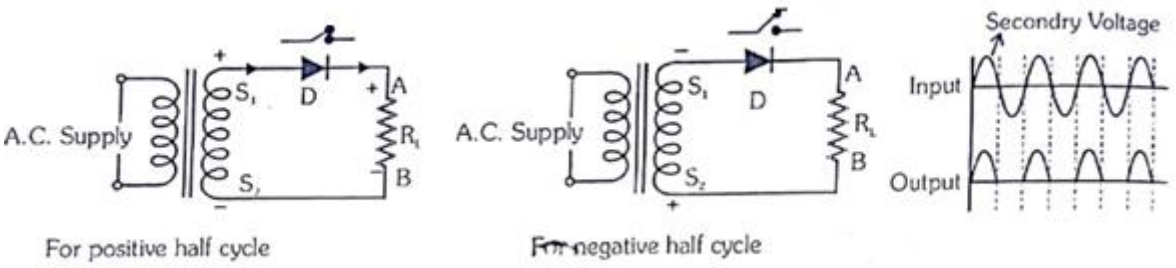
Comparison between forward and reverse bias

S.No.	Forward Bias	Reverse Bias
1.	Potential Barrier reduces and width of depletion layer decreases.	Potential Barrier increases and width of the depletion layer Increases.
2.	P–N junction provides a very small resistance.	P–N junction provides high resistance.
3.	Forward current flows in the circuit and order of current is milliamperes.	Very small current flows and order of current is microampere.
4.	Current flows mainly due to majority carriers.	Current flows mainly due to minority carriers.
5.	Forward characteristic curve 	Reverse characteristic curve 
6.	$R_t = \frac{\Delta V_t}{\Delta I_t} \cong 100\Omega$ Forward resistance	$R_t = \frac{\Delta V_t}{\Delta I_t} \cong 10^6\,\Omega$ Reverse resistance

Rectifier

Rectifier is the device which is used for converting alternating current into direct current.

Half wave rectifier- In half wave rectifier, half part of the alternating current is rectified.

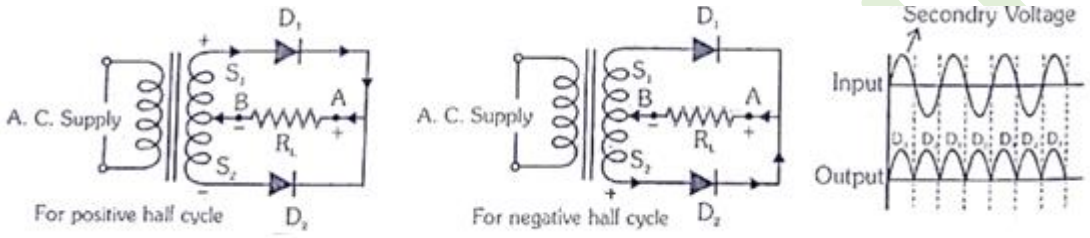


During the first half (positive) of the input signal, let S_1 is at positive and S_2 at negative potential. So the PN junction diode D is forward blessed. The current flows through the load resistance R_L and output voltage is obtained.

During the second half (negative) of the input signal, S_1 and S_2 would be negative and positive respectively. The PN junction diode will be reversed biased. In this case, practically no current would flow through the load resistance. So, there will be no output voltage.

Peak inverse voltage (PIV)- In half wave rectifier PIV = maximum voltage across the secondary coil of the transformer (V_S) = Peak value of output (V_m)

Full wave rectifier- In a Full Wave Rectifier circuit, two diodes used, one for each half of the cycle.



When the diode rectifies the whole of the AC wave, it is called full rectifier. Figure shows the experimental arrangement for using diode as full wave rectifier. The alternating signal is fed to the primary a transformer. The output signal appears the load resistance R_L.

During the positive half of the input signal: Let S_1 positive and S_2 negative. In this case diode D_1 is forward biased and D_2 is reverse biased. So only D_1 conducts and hence the flow of current in the load resistance R_L is from A to B.

During the negative half of the input signal: Now S_1 is negative and S_2 positive D_1 is reverse – biased and D_2 is forward biased. So only D_2 conducts and hence the current flows through the load resistance RL from A to B. It is clear that whether the input signal is positive or negative, the current always flows through the load resistance in the same direction and wave rectification is obtained.

Form Factor- It is the ratio of rms current to dc current, $F = \frac{I_{rms}}{I_{dc}} or \frac{E_{rms}}{E_{dc}}$

$$F = \frac{\pi}{2\sqrt{2}}$$

for full wave rectifier

$$F = \frac{\pi}{2}$$

for half wave rectifier

Ripple and ripple factor- In the output of the rectifier, some A.C. components are present. They are called ripple & there measurement is given by a factor known as the ripple factor. For a good rectifier, ripple factor must be very low.

Total output current $I_{rms} = \sqrt{I^2_{ac} + I^2_{de}}$

Where I_{ac} = rms value of AC component present in the output

Ripple factor= $r = \frac{I_{ac}}{I_{dc}} \Rightarrow r = \sqrt{\frac{I^2_{rms}}{I^2_{dc}} - 1} = \sqrt{F^2 - 1}$

Rectifier efficiency = $\eta = \frac{P_{dc}}{P_{ac}} = \frac{I^2_{dc}\ R_L}{I^2_{rms}\ (R_F + R_L)}$

Zener Diode

A specifically doped crystal diode which can work break down region is known as Zener diade. It is always connected in reverse biased. In forward biased, it works as a simple diode.

Symbol of Zener diode 

Transistor

A transistor is a three terminal device which transfers a signal from a low resistance circuit to high resistance circuit. It is formed when a thin layer of one type of extrinsic semiconductor (P or N-type) is sandwiched between two thick layers of other types of extrinsic semiconductor. Each transistor have three terminals which are

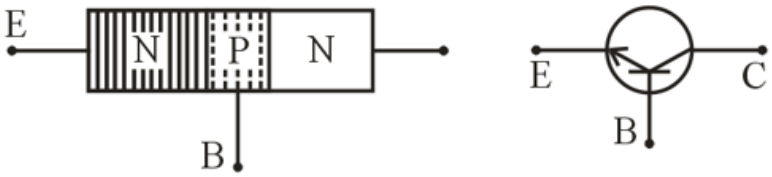
Emitter : It is the left most part of the transistor. It emits the majority carrier towards the base. It is highly doped and medium in size.

Base: It is the middle part of the transistor which is sandwiched by emitter € and collector (C). It is lightly doped and very thin in size.

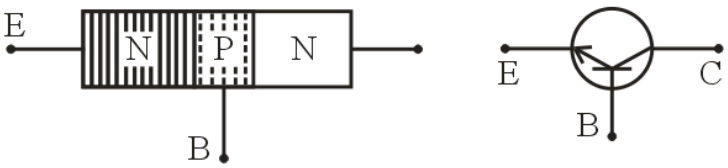
Collector: It is right part of the transistor which collects the majority carriers emitted by the emitter. It has large and moderate doping.

There are two types of transistor

NPN Transistor: If a thin layer of P-type semiconductor is sandwiched between two thick layers of N-type semiconductor is known as NPN transistor.

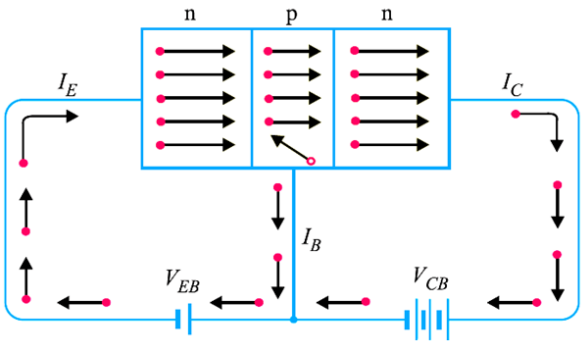


PNP Transistor: If a thin layer of N-type of the semiconductor is sandwiched between two thick layers of P-type semiconductor is known as PNP transistor.



Working of NPN Transistor

Given that the emitter Base junction is forward bias and the collector-base junction is reversed biased of n–p–n transistor in the circuit shown in Figure.



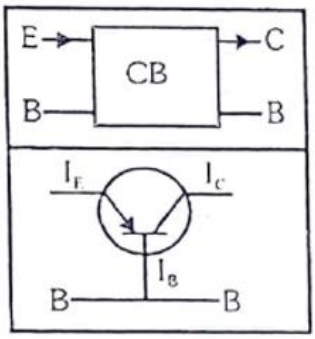
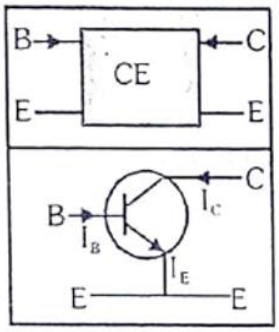
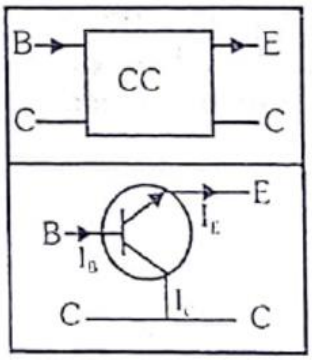
When the emitter-base junction is forward bias electrons (majority carriers) in emitter in are repelled toward the base. The barrier of emitter-base junction is reduced and the electron enters the base, about 5% of these electrons recombine with the hole in base region result in small current (I_b).

The remaining electron (»95%) enter the collector region because they are attracted to the positive terminal of the battery. For each electron entering the positive terminal of the battery is connected with collector-base junction an electron from the negative terminal of the battery connected with emitter-base junction enters the region.

The emitter current (I_e) is more than the collector (I_c). The base current is the difference between I_e and I_c and proportional to the number of electron hole recombination in the base.

$I_e = I_b + I_c$

Comparison of different types of transistor configurations

Properties	**Common Base transistor (CB)**	**Common Emitter Transistor (CE)**	**Common Collector Transistor (CC)**
			
Input Resistance	**Low**	**High**	**Very High**
Output resistance	**Very High**	**High**	**Low**
Current Gain	(A_I or α) $\alpha = \frac{I_C}{I_E} < 1$	(**A_I** or β) $\beta = \frac{I_C}{I_E} > 1$	(A_I or g) $\gamma = \frac{I_E}{I_B} > 1$
Voltage Gain	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_E I_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_B I_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_E R_L}{I_B I_i}$
Power Gain	$A_p = \frac{P_o}{P_i}$ $A_p = \alpha^2 \frac{R_L}{R_i}$	$A_p = \frac{P_o}{P_i}$ $A_p = \beta^2 \frac{R_L}{R_i}$	$A_p = \frac{P_o}{P_i}$ $A_p = \gamma^2 \frac{R_L}{R_i}$
Phase difference (between output and input)	Same phase	Opposite phase	Same phase

Relation Between α, β, and γ

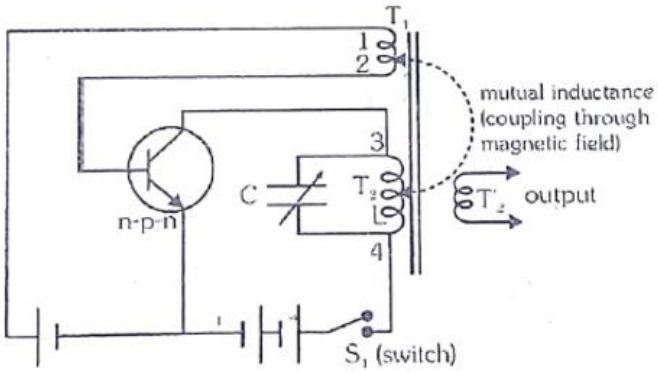
$$\beta = \frac{\alpha}{1-\alpha}, \quad \gamma = \frac{1}{1-\alpha}, \text{ and } \quad \gamma = 1+\beta$$

Transistor as an Oscillator

An oscillator is a device which delivers a.c. output wave from of desired frequency from d.c. power even without input signal excitation.

The electric oscillations are produced by LC circuit (i.e tank circuit containing inductor and capacitor). The amplitude of oscillation decreases with the passage of time due to the small resistance of the inductor or the energy of the LC oscillations decreases. If this loss of energy is compensated from outside, then undamped oscillations (of constant amplitude) can be obtained. This can be done by using feed back arrangement and a transistor in the circuit.

LC circuit producing LC oscillations consist of an inductor of inductance L and capacitor of variable capacitance C inductor which is connected in the collector-emitter circuit through a battery and tapping key (K).



The resonant frequency of an LC oscillator is,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Logic gate

A logic gate is a digital circuit which is based on the certain logical relationship between the input and the output voltage of the circuit.

The operation of a logic gate is indicated in the table known as a truth table. This table contains all possible combinations of inputs and the corresponding outputs.

A logic gate is also represented by a Boolean algebraic expression. Boolean algebra is a method of writing logical equations showing how an output depends upon depends upon the combination of inputs. Boolean algebra was invented by George Boole.

Basic Logic Gates

OR gate- In OR gate the output of an OR gate attains the state 1 if one or more inputs attain the state 1 .

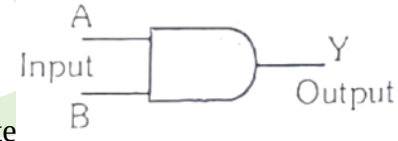
Logic symbol of OR gate 

The Boolean expression of OR gate is Y = A + B, read as Y equals A 'OR' B.

The truth table of a two-input OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

AND gate- In AND gate the output of an AND gate attains the state 1 if and only if all the inputs are in state 1.

Logic symbol of AND gate 

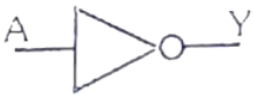
The Boolean expression of AND gate is Y = A.B

The truth table of a two-input AND gate

A	B	Y
0	0	0

0	1	0
1	0	0
1	1	1

NOT gate- In NOT gate the output of a NOT gate attains the state 1 if and only if the input does not attain the state 1.

Logic symbol of NOT gate 

The Boolean expression is $Y = \overline{A}$, read as Y equals NOT A.

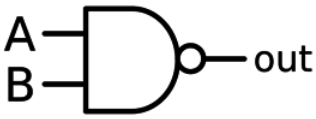
The truth table of NOT gate

A	Y
0	1
1	0

Combination of gates

The three gates (OR, AND and NOT), when connected in various combinations, give us logic gates such as NAND, NOR gates, which are the universal building blocks of digital circuits.

NAND gate- This gate is the combination of AND and NOT gate.

Logic symbol of NAND gate 

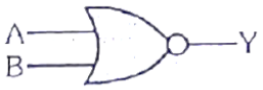
The Boolean expression of NAND gate is $Y = \overline{A.B}$

The truth table of a NAND gate

A	B	Y
0	0	1
0	1	1

1	0	1
1	1	0

NOR gate- This gate is the combination of OR and NOT gate.

Logic symbol of NOR 

The Boolean expression of NOR gate is $Y = \overline{A + B}$

The truth table of a NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Exclusive-OR gate (XOR gate):- In XOR gate the output of a two-input XOR gate attains the state 1 if one add only input attains the state 1.

Logic symbol of XOR gate 

The Boolean expression of the XOR gate is $Y = A\bar{B} + \bar{A}B$ or $Y = A \oplus B$

Truth table of an XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive-NOR gate (XNOR gate)- In XNOR gate the output is in state 1 when its both inputs are the same that is, both 0 or both 1.

Logic symbol of XNOR gate 

The Boolean expression of XNOR gate $Y = A.B + \overline{A}\,\overline{B}$ or $Y = \overline{A \oplus B}$ or $A \oplus B$

Truth table of an XNOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

De Morgan's theorem

First theorem- It states that the NAND gate is equivalent to a bubbled OR gate.

$$\overline{A.B} = \overline{A} + \overline{B}$$

Second theorem- It states that the NOR gate is equivalent to a bubbled AND gate.

$$\overline{A + B} = \overline{A}.\overline{B}$$

All the best!

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